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DEVELOPMENT OF A 4-BIT FLASH ANALOG-TO-DIGITAL CONVERTER USING CMOS VLSI 180nm FULL CUSTOM TECHNOLOGY

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Abstract – Analog to digital converters are widely used in all kinds of areas since they can ensure a communication between the computer and the external world, the development of a 4-bit A/D flash type converter as the main objective for this article follows the same purpose. The paper was planned in a way that, with a great number of tables and graphs, most people would be able to understand and replicate the desired results correctly. The simulation, which is the main part of the development of the article, was done using a software called LTSpice, a program with several tools and components that made possible to assemble a converter, besides that, the software also has a tool that allows to create new components, in which it was developed full custom AND and OR logic gates based on CMOS technology. At last, the results show satisfactory graphs that prove the functioning of the converter.

Keywords: A/D Converter; LTSpice; CMOS; Full Custom; 4 bits;

INTRODUCTION

Most magnitudes in nature are analog, therefore, to enable the processing of these signals in digital systems, it is necessary to use an analog-to-digital (A/D) converter [1]. Many types of analog signals are present in nature, among them, some examples that can be cited are: temperature, humidity, pressure, audio signals, light intensity and others [2].

A A/D converter, also known as ADC (Analog-to-Digital Converter), consists on a circuit that receives an alternating voltage signal at the input and, after a certain time, it converts that signal into a digital corresponding binary code [2],[3]. Several areas use these types of converters in their equipment, some examples would be the instrumentation area (which uses it for oscilloscopes, digital multimeters, spectrum analyzers and more), the telecommunications area (that uses it for terrestrial communication or satellite communication), communication systems (such as cell phones), medical examinations (by image, radars and others) and many more fields [2], [3], [4].

There are many types of circuits that can perform the conversion of an analog signal into a digital binary code, each one of them with their own advantages and disadvantages. Between those circuits, can be cited:

- Digital ramp ADC;
- Dual ramp ADC;
- Successive approximation ADC;
- Flash ADC (also known as parallel topology ADC);

Knowing the importance of these converters, this work presents the development and simulation of a 4-bit flash analog-to-digital converter using the software LTSpice. Although many comparators are needed to build this circuit (in this case, 15 analog comparators), this topology was chosen for having a higher ADC conversion speed [2].

DEVELOPMENT

For the development of this project, the researchers chose the simulation software called LTSpice, in which it was used the components of the foundry CMOS Mosis Wafer Electrical Foundry IBM

7WL_4LM_ML_HK 180 nm together with the library of CMOS logic gates and the libraries developed by the authors. Fig. 1 represents the architecture of a flash converter N bits.

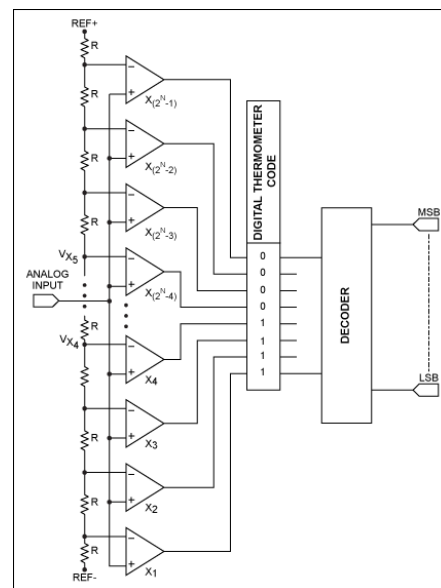


Figure 1: Structure of an N-bit flash converter [5].

The operations realized in this converter can be divided in three steps: tension division (responsible to create reference tensions), comparison and codification. In the first step, a reference tension (in this case, something around 10V) on a tension divisor that will generate 15 levels of tension (each one with a 0,34V tension).

On the second step, each one of the reference tensions are connected to the inverter port of a operational amplifier (AD549), which will play the role on comparing these reference voltages with an analog voltage (in this case, a 15kHz sine wave that has an amplitude of 2.9V and a DC value of 6.5V). When the value of this sine wave is greater than the reference voltage, the op-amp output will be on high



logic level (approximately 8.5V), otherwise the output will be on low logic level (approximately 0V).

After the comparison, the output signals of each operational amplifiers will go through a priority encoder, which aims to transform this signal into its binary counterpart. To perform this conversion, AND and OR logic gates developed with VLSI full custom technology were used.

On developing the priority encoder, it is initially necessary to associate each one of the OPAMPs outputs possibilities to various AND gates, generating

all 16 possible outcomes. This can be seen in Table 1, where, using “1” as high logic level and “0” as low logic level, it is possible to check the relation between the logic levels of the comparators and the AND gates outputs in each case (excluding Output 16, or “S16”, because it is a logic gate that only will provide a high logic level when all comparators are at a low logic level).

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 1: Relation between the output of OP AMPs and the inputs of AND gates.

In order to build a 15-input AND gate, it was initially necessary to build a CMOS circuit to a NAND gate, which consists of a pullup network composed of 15 PMOS transistors connected in series and a pull-down network composed of 15 NMOS transistors connected in parallel. when all inputs are at low logic level, all PMOS transistors will start to conduct, in that way, the port output will be 1 and, if any of the 15 inputs becomes high logic level, the gate output will

be 0. Now, to obtain an AND gate, it is necessary connect the NAND gate output to an inverter, which consists of a pull-up network composed of a PMOS transistor and a composite pull-down network composed by a NMOS transistor. To build all AND gates it was required a total of 512 transistors. The Figure 2 shows the developed logic gate circuit.

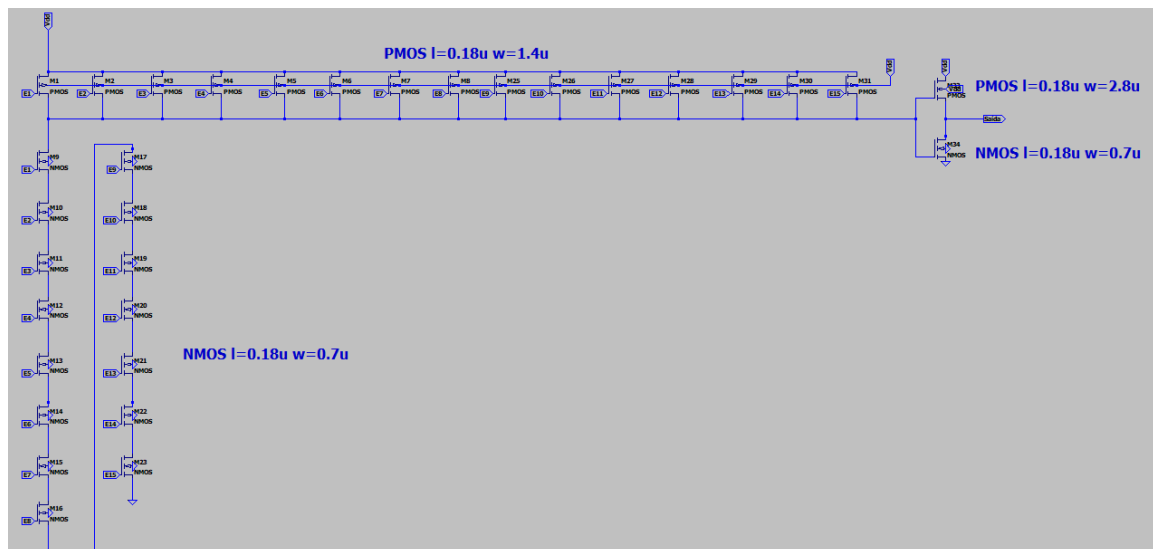


Figure 2: AND gate CMOS circuit.



The developed component features a time rise and a time fall of approximately 33 ns. In addition to that, the developed component also presents a current of operation of 3mA for a 1 kΩ load.

After the coding stage, it is necessary to transform each one of the AND gates outputs into its binary counterpart. For this, it was used OR logic gates, which will only provide a high logic level when one of its inputs also provides a high logical level. This

relation, along with all possibilities can be verified in Table 2.

S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	D0	D1	D2	D3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Table 2: Relation between AND gate outputs and OR gate outputs.

For the development of an 8-input OR gate, it was initially necessary to develop a NOR gate. For this, a pull-up network composed of 8 PMOS transistors were connected in series and a pull-down network consisting of 8 connected NMOS transistors were connected in parallel. When all entries are in low logic level, all the PMOS transistors will start to conduct, in that way, the output from the gate is at high logic level

“1”. But when one of the inputs is at a high logic level, the transistors NMOS will start to conduct, and then the output of the gate will be at low logical level “0”. In order to obtain a OR gate, it is necessary to connect the output of the NOR gate to an inverter. To build all the OR gates it was necessary a total of 72 transistors (totaling 584 transistors for building all logical gates). Figure 3 shows the developed logic gate circuit.

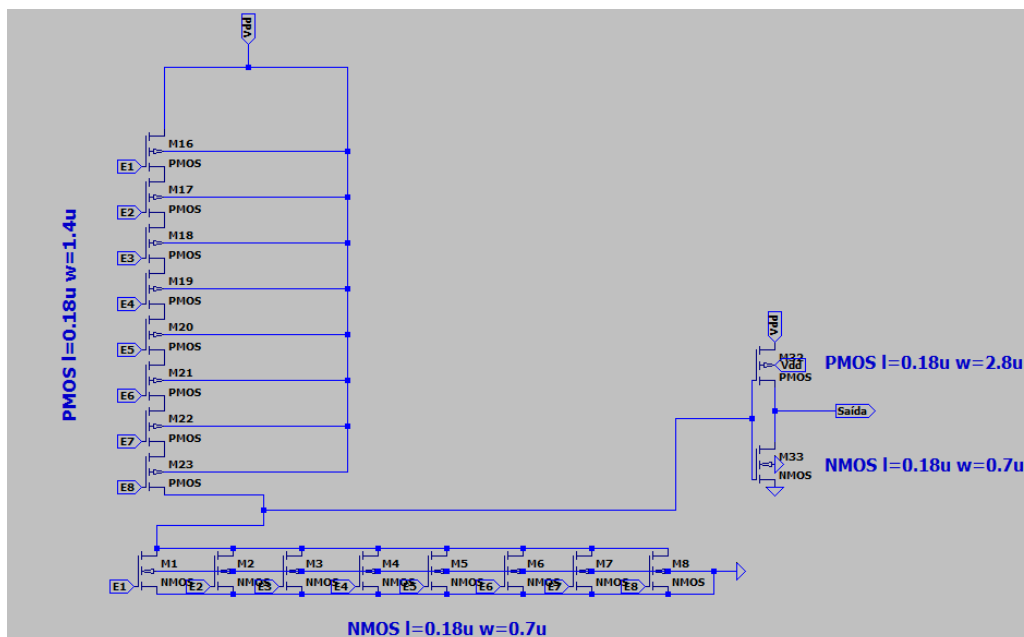


Figure 3: OR gate CMOS circuit.



The developed component features a time rise and a time fall of approximately 5.5 ns. In addition, the developed component also presents a current of operation of 3 mA for a 1 k Ω load.

After the simulation was done, it was possible to obtain the graphs containing the voltage levels generated in the voltage divider, and the output of operational amplifiers. Fig. 4 show these results obtained in the simulation.

RESULTS AND DISCUSSION

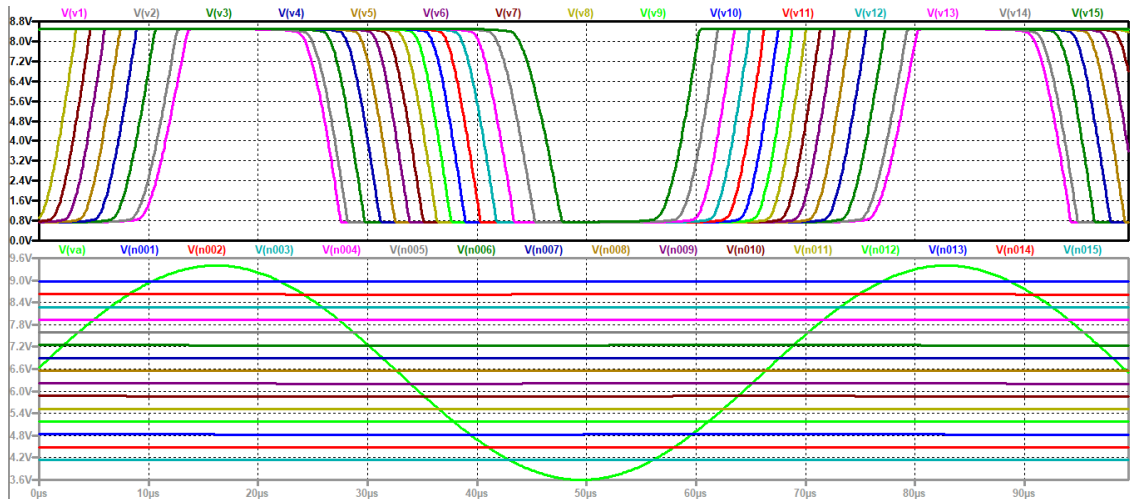


Figure 4: Relação entre tensão de entrada e saída dos AMPOPs.

As can be observed in Fig. 4, the voltage step generated in the voltage dividers is approximately 0.34V, which means that, in order to change the digital output of the converter, it is necessary to change by 0.34V the analog input voltage. With that, it is possible to observe that as the analog voltage increases, more operational amplifiers have the output at a high logic level, reaching a point where the input voltage becomes greater than the output voltage on the highest reference tension, making all OPAMPs outputs high logic level. However, as the analog voltage starts to decrease, the OPAMPs outputs start to become low logic level, until the analog voltage becomes lower

than the lowest reference tension, causing all OPAMPs outputs to become low logic level.

With this data, it was possible to obtain the digital output of the proposed converter. The Fig. 5 presents the relationship between analog input voltage and output converter digital.

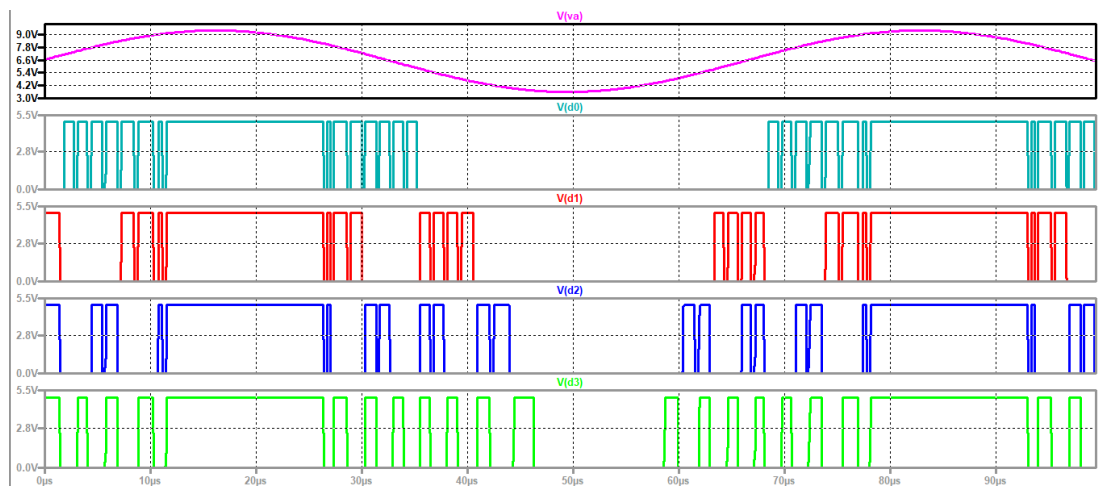


Figure 5: converter digital output.

Following the graphs in Fig. 5 it was possible to obtain the values in Table 3, which show the relation between the voltage ranges at the input of the converter with its digital output. It is worth noting that D0 is the most significant bit.



Tensão de entrada (V)	D0	D1	D2	D3
3,60 – 4,14	0	0	0	0
4,14 – 4,48	0	0	0	1
4,48 – 4,82	0	0	1	0
4,82 – 5,16	0	0	1	1
5,16 – 5,50	0	1	0	0
5,50 – 5,84	0	1	0	1
5,84 – 6,18	0	1	1	0
6,18 – 6,52	0	1	1	1
6,52 – 6,86	1	0	0	0
6,86 – 7,20	1	0	0	1
7,20 – 7,54	1	0	1	0
7,54 – 7,88	1	0	1	1
7,88 – 8,22	1	1	0	0
8,22 – 8,56	1	1	0	1
8,56 – 8,90	1	1	1	0
> 8,90	1	1	1	1

Table 3: Relation between input voltages and digital outputs.

Better Analyzing the graphs on Fig. 5, it is possible to notice that there are certain voltage peaks, called ripple, in which, due to the intrinsic characteristics of the component, they appear several times in all the “digital outputs”. In order to remove them, a filter can be used at the output of each OR gates, thus eliminating the frequencies that generate by these ripples.

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ANALYSIS OF THE EFFECTS OF ELECTROMAGNETIC RADIATION ON PLANTS DEVELOPMENT

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Abstract – The population growth of the last decades has created the need to look for new ways to increase the productivity of crops. Knowing this, several studies began to be carried out in order to analyze the influence of electromagnetic radiation on the development of plants. With that in mind, the present work presents an experiment carried out to analyze the influence of the irradiation of an electromagnetic wave of 2.3625 GHz in the development of a corn crop by comparing the growth of this plant exposed to this extra radiation with another that is only exposed to the ambient radiation. The results demonstrate that the plant exposed to the radiation set at a specified frequency has a decrease in root size.

Key-Words: Electromagnetic radiation; Development; Corn; Root;

INTRODUCTION

Due to the exponential growth of the world population over the last centuries, the need for technological advances aimed at agriculture to satisfy the needs has been constant. And this is no different today, with a forecast of 8 billion inhabitants for 2025 and 9 billion for 2050, the need arises to study new more sustainable agriculture techniques, which increase the productivity of crops and use less and less water and energy resources [1].

Over the last few decades, several experiments have been carried out to identify the benefits that the exposure of plants to electromagnetic radiation could cause. Some of these studies presented data that show a relationship between plant growth and the time it is exposed to electromagnetic radiation. According to these researches, keeping the plant exposed to electromagnetic radiation for a certain time results in a chance of increasing the growth capacity of the crop. However, if the test subject gets irradiated for too long, there is a decrease in the germination capacity of the plant [2]. This relationship can be seen in Fig. 1.

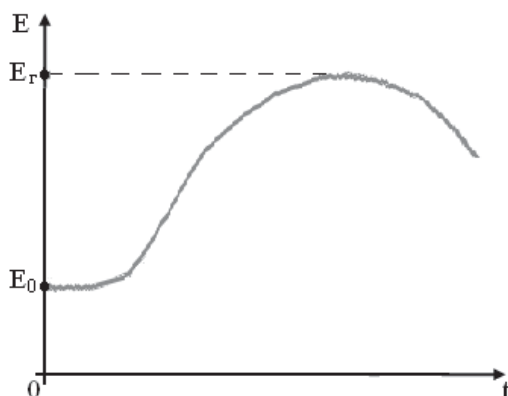


Figure 1: Relationship between the time of exposure to electromagnetic radiation with plant growth [2].

Besides the time the plant is exposed to electromagnetic radiation, certain studies have shown that the frequencies of these waves can cause different effects on its development. [3]. The Table 1 shows some effects caused by different frequencies.

Frequência	Fenômeno observado
60-100 Hz	Produção de alalina
400, 900, 1900 MHz	Crescimento e alterações bioquímicas
900 MHz	Desenvolvimento da planta
2.4 GHz	Produção de metabólitos secundários
53.6 GHz	Maior germinação

Table 1: Observed phenomena for different frequencies [3]

These relations can be observed in a study carried out in 2005, in which the author of the research, plants *lemna minor* (also known as duckweed) and leaves it exposed to electromagnetic waves of 400 MHz and 900 MHz (both with field 23, 41 and 390 V/m) for two hours daily for 3, 5, 8, 10, 12 and 14 days. At the end of the experiment, it was observed that there was an increase of approximately 15% in the growth capacity of the plant exposed to a wave of 400 MHz, electric field of 23 V/m, exposed for two hours a day over three days. On the other hand, in other cases, it was possible to observe a reduction in the plant's growth capacity [4].

As shown in the research cited above, different frequencies cause different effects on plants. Some other studies carried out more recently, had data that also pointed support to this fact. A work carried out in 2007 presents data regarding the irradiation of an alternating magnetic field of a wave of 50Hz, in these data it is possible to perceive that there was an increase in the yield of the beet roots [5]. Another study carried out in 2021, pointed out a phenomenon that happened in a forest near a village in Turkey in which the vegetation near a radio tower located in this forest was extremely negatively affected by the electromagnetic fields generated in that tower. In this research, as they got closer and closer to the tower, the vegetation was gradually reduced due to the high exposure of the radiation generated by the radio tower [6]. This graphic relationship between the number of plants



present and the distance from the tower can be seen in Fig. 2.

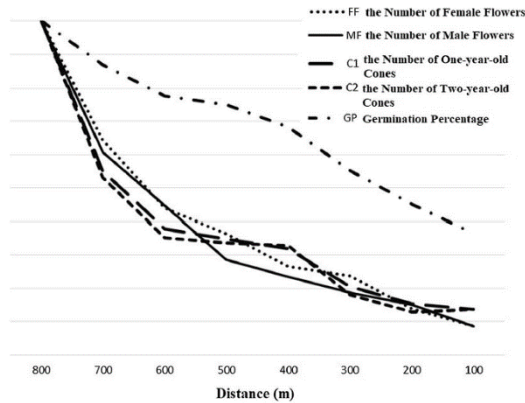


Figure 2: Graphic representation of the number of plants with the distance from the tower [6].

Knowing these facts discussed above, the present experiment proposes to analyze the influence of exposure to electromagnetic radiation on the development of corn, observing the positive or negative influences that may occur according to the time in which the corn is exposed to radiation.

DEVELOPMENT

To carry out this experiment, two cultures of *zea mays*, also known as corn corn (QUALITÁ-Alnutri Alimentos Ltda.), were planted in Styrofoam pots filled with soil, as shown in Fig. 3, where one of the cultures was exposed to electromagnetic radiation for two hours a day for five days, while the other culture was exposed only to ambient electromagnetic radiation. The corn used is distributed by the company GPA and its lot is 0000024206.



Figure 3: Cultures of *zea mays*, the top one was considered the "control" and the bottom one the "radiated".

In addition, cultures were watered daily with 25 mL of mineral water (CRYSTAL-Spal Indústria Brasileira de Bebidas S.A.) which, at 25°C, has a pH of 7.49, conductivity of 204 $\mu\text{S}/\text{cm}$ and evaporation residue at 180°C of 160.70 mg/L. In addition, its composition has 131.77 mg/L of NaHCO_3 , 43.561 mg/L of Na^+ , 4,698 mg/L of Ca^+ , 2,503 mg/L of K^+ , 1,94 mg/L of Cl^- , 1,233 mg/L of Mg^+ , 1 mg/L of F^- , 0,98 mg/L of SO_4^{2-} , 0,68 mg/L of PO_4^{3-} , 0,144 mg/L of Ba, 0,053 mg/L of B, 0,050 mg/L of Sr, 0,035 mg/L of Fe and 0,03 mg/L of NO_3^- .



Figura 4: Água e Milho utilizados.

To carry out the electromagnetic bombardment, a timer was used that has the function of turning a microwave generator on and off, which was set to work for a period of 2 hours a day. This equipment can be seen in Fig.5.



Figure 5: timer used in the experiment.

In addition, for the purpose of also radiating the electromagnetic waves to the ground, a signal generator and a patch-type antenna were used. The system assembled with these devices can be seen in Fig. 6. The signal generator used generates a wave of approximately 2.3625 GHz, as represented in the radiation diagram of Fig.7.

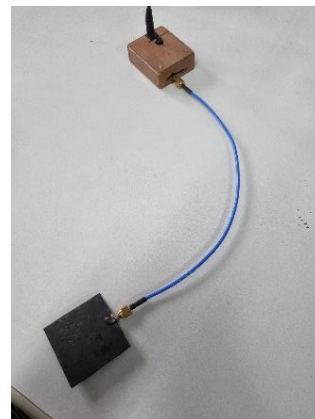


Figure 6: system used to irradiate the soil.

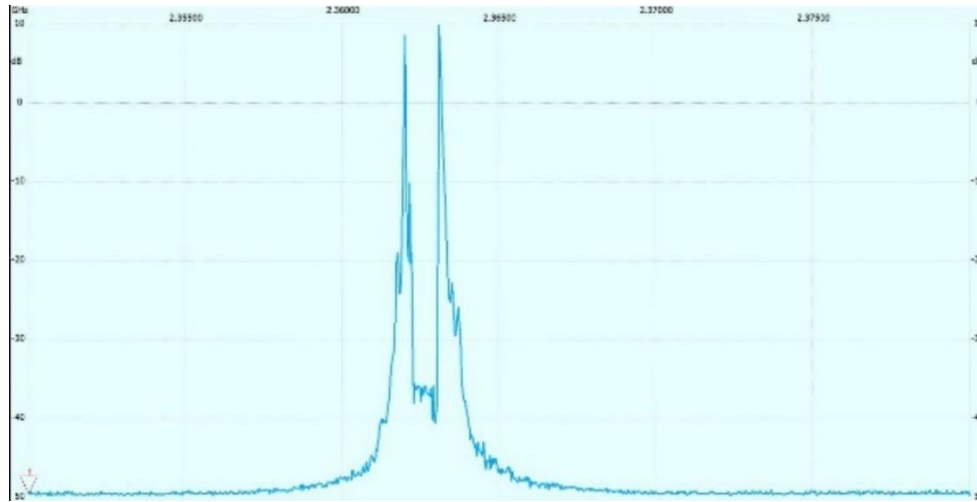


Figure 7: Microwave generator radiation diagram.

RESULTS AND DISCUSSION

The experiments were carried out under the following conditions, two separate Styrofoam pots were filled using land from the same source, and within each of them, five seeds were planted in order to increase the chance of successful germination. One of the soil amounts was irradiated for two hours a day over five days, and after that, it was waited another five days for both the irradiated and the control to develop.

During the experiment, it was possible to observe some effects that the electromagnetic radiation radiated on the corn seeds caused after ten days of growth, however, for an experiment to be complete it would be necessary to observe a frequency in the results. For this, the same procedure was performed three times, in the same place with very similar luminosity (measured with the aid of a luxmeter).

After the first ten days, the plants were removed from their land and their growth compared to the control plant could be observed, as shown in Fig. 8 and 9.



Figure 8: Length of plant irradiated with micro-waves in experiment

1



Figure 9: Control plant length in experiment 1

This measurement was carried out with all the seeds of the experiment, comparing the size of the control plants with the irradiated ones, and in this experiment, it can be seen that speaking in terms of average, the roots of the control plants are larger than the irradiated ones, and they presented a better growth. In this case, taking the best developed ones from each pot, a difference of approximately 2 cm can be observed in their roots, where the one without radiation had 28 cm and the plant exposed to radiation approximately 26 cm.

To continue the experiment, the same event was performed again, and after another ten days the results presented in Fig. 10 and 11.



Figure 10: Length of plant irradiated with micro-waves in experiment 2



Figure 11: Control plant length in experiment 2

Again, it is possible to observe a pattern in the terms of the root size of plants without radiation being significantly larger than those with radiation, considering the measured values: 23 cm with radiation and 29 cm without radiation (rounding was used in the measurements since the roots of plants are not perfectly straight and too fragile for us to force them straight).

To guarantee the thesis, another experiment was carried out, using the same patterns previously followed. The results obtained can be seen in Fig. 12 and 13.



Figure 12: Length of plant irradiated with micro-waves in experiment 3



Figure 13: Control plant length in experiment 3

It can be seen that the pattern was maintained in these roots, and although this experiment had the same period of 10 days, the climate was less favorable for the growth of the plant in question (low temperatures), but even so, the growth of the two plants is shown to be with the same equivalence pattern where the plant with radiation has 11 cm of roots, and the one without

radiation has 15 cm, being able to observe the obviously influence in the growth of the plant.

The results obtained made possible to conclude that the electromagnetic waves caused the roots to suffer a negative influence on their growth, but an interesting point to highlight is that despite the delayed development of the roots, their growth as a plant remained on par with the same the control plant.

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DEVELOPMENT OF A SWR METER USING MICROSTRIP LINES

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Abstract – This paper presents, in a summarized manner, the development and simulation of a standing wave ratio meter using the Quite Universal Circuit Simulator Studio (QucsStudio) software. The selected substrate for the project was FR-4.

Keywords: Standing wave ratio meter; QucsStudio; FR-4.

INTRODUCTION

Wireless transmissions are of great importance in various areas of development. Antennas form the basis of wireless transmissions [1]. For optimal performance of these antennas, impedance matching is necessary. In a real scenario, there is a possibility of energy transfer problem between the line and the antenna [2]. Standing wave refers to the periodic oscillation that occurs in propagated frequency waves. An alternative, with excellent cost-effectiveness, is the use of standing wave ratio meters.

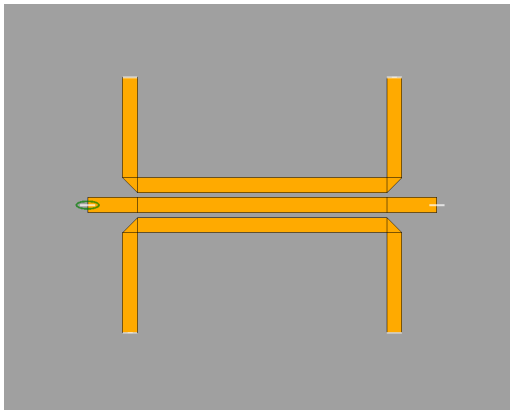


Figure 1 – Printed circuit SWR meter

The device under analysis was developed based on a model [5], using the QucsStudio software.

DEVELOPMENT

Parameters were inserted to study the circuit behavior across the range of 120 MHz to 500 MHz. In addition to the behavior, the main characteristic of this device was also observed: the impedance matching verification within a range of 0 to 100Ω through Rsweep (device output). With that said, P1 (device input) is considered as another device (such as a coaxial cable) with 50Ω impedance. The circuit compares, among the given frequencies and the impedances of Rsweep, where the best impedance match with P1 occurs.

Directional couplers must fulfill another characteristic of an SWR meter: the transmission line must have a null external field [3]. In other words, the diode of each directional coupler needs to be biased in a way that only signals occurring in one direction are measured. One diode is responsible for the reflection half-cycle (vref), and the other is responsible for the incident (v fwd) signals.

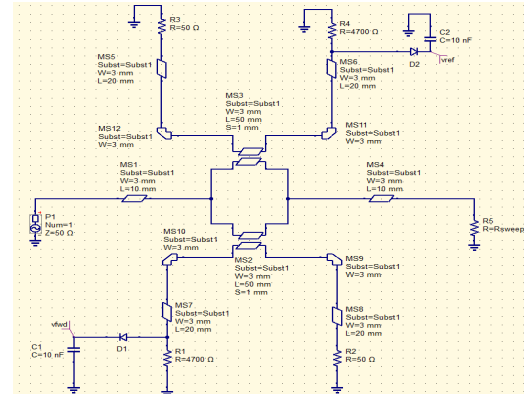


Figure 2 – SWR meter circuit in QucsStudio.

RESULTS AND DISCUSSIONS

Using the parameters presented in the previous figure, the simulation was performed. At the end of it, the following diagram was obtained:

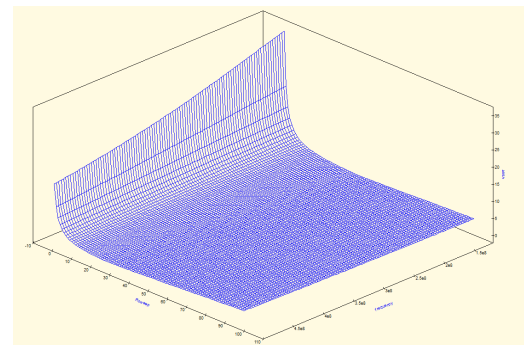


Figure 3 – SWR meter circuit in QucsStudio

Observing the diagram, it is noticeable that the VSWR is low when Rsweep is equal to 50Ω. It is also noted that the VSWR increases as Rsweep deviates from 50Ω because this is the value present at P1, indicating optimal impedance matching. Finally, it can be observed that when attempting a match with 0Ω, the VSWR assumes extremely high values. This occurs because all the signal being sent ends up being reflected back to the source P1 (damaging the entire circuit). Lastly, another point to highlight is that,